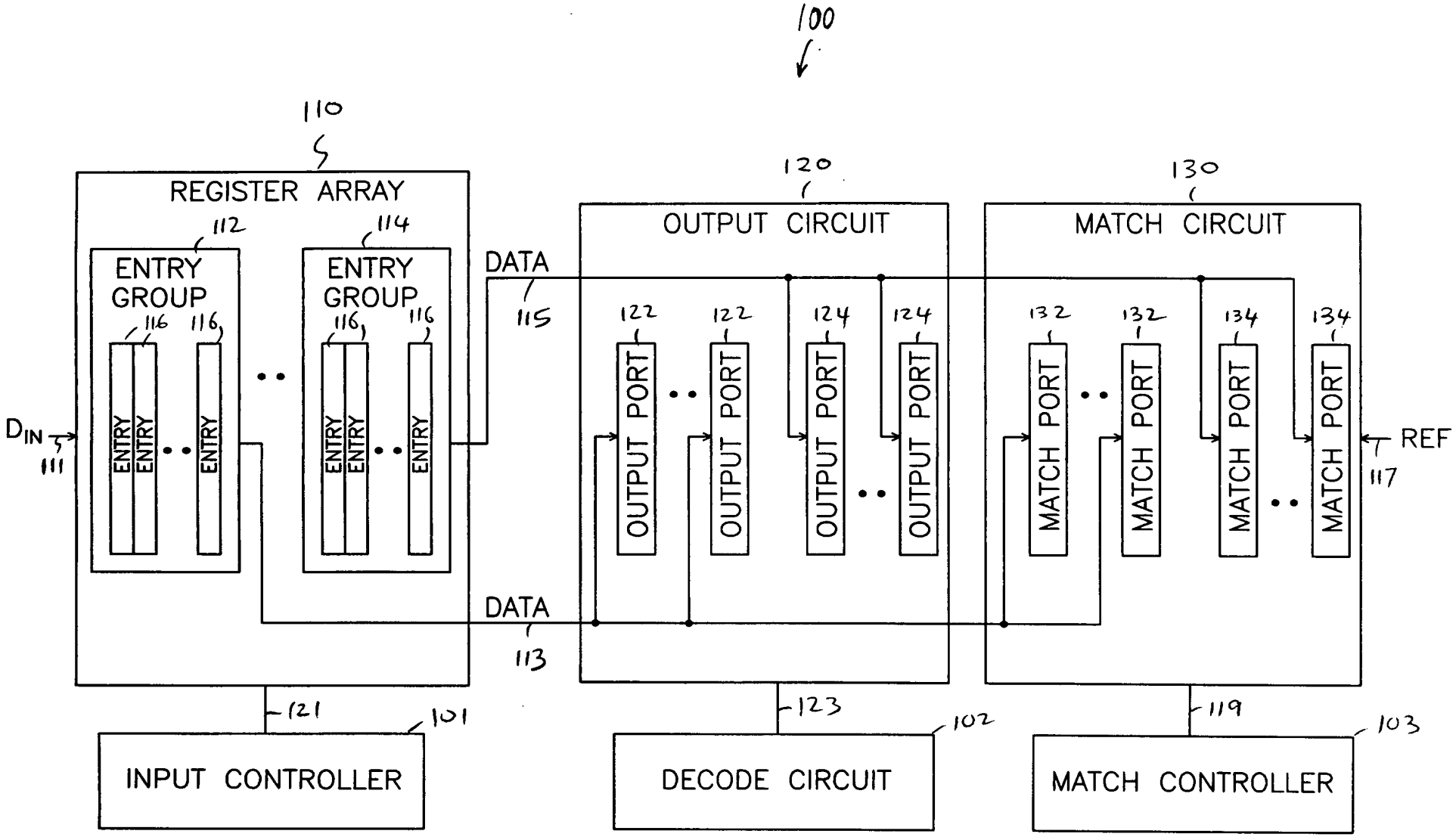

100
110
REGISTER ARRAY
112
114
ENTRY GROUP
ENTRY GROUP
116
ENTRY
D_{IN}
111
DATA
115
120
OUTPUT CIRCUIT
122
124
OUTPUT PORT
130
MATCH CIRCUIT
132
134
MATCH PORT
REF
117
DATA
113
121
101
INPUT CONTROLLER
123
102
DECODE CIRCUIT
119
103
MATCH CONTROLLER

FIG. 1

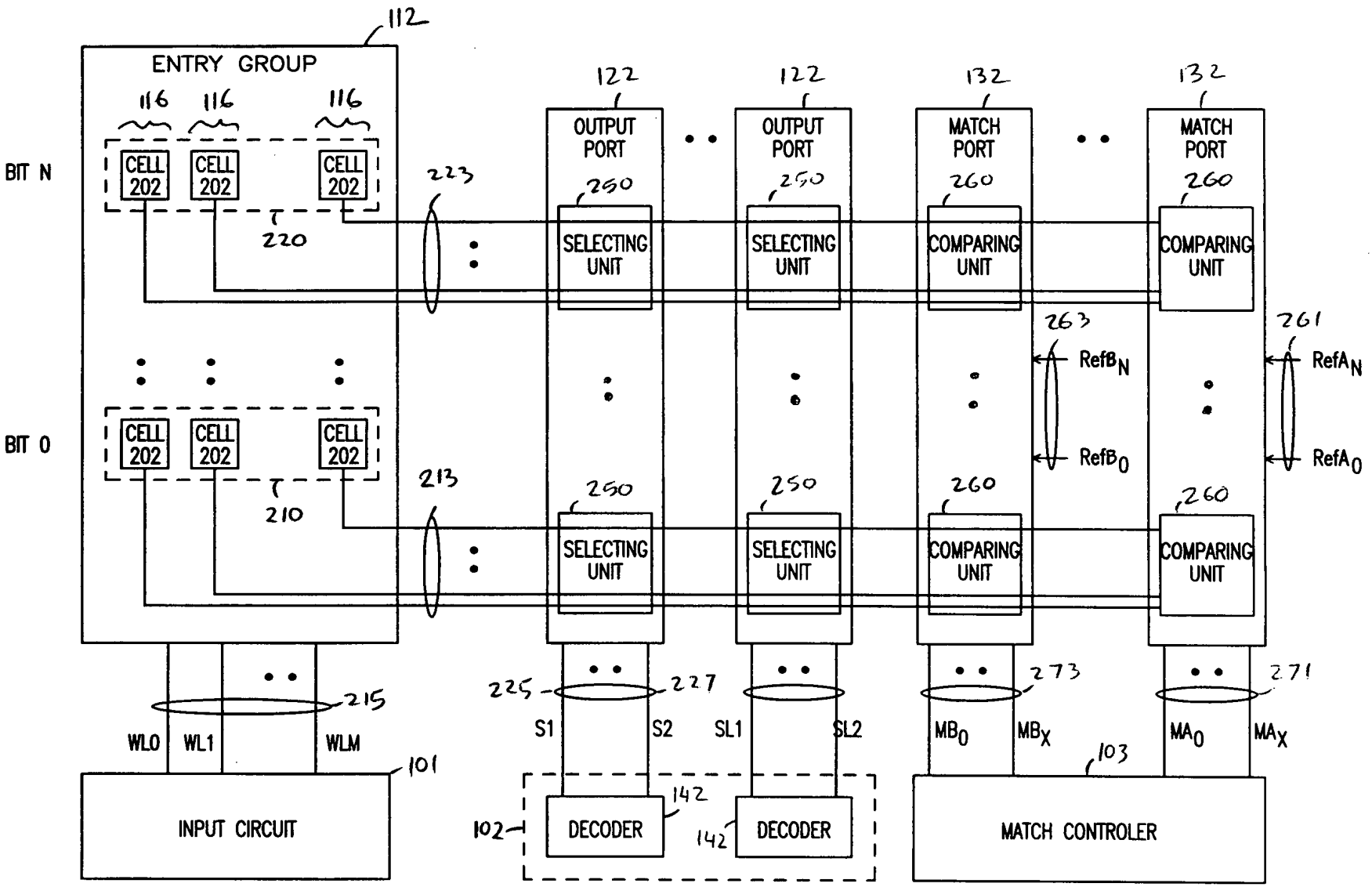

112
ENTRY GROUP
116
116
116
BIT N
BIT 0
CELL 202
CELL 202
CELL 202
CELL 202
CELL 202
CELL 202
220
210
223
213
122
122
OUTPUT PORT
OUTPUT PORT
250
250
SELECTING UNIT
SELECTING UNIT
SELECTING UNIT
SELECTING UNIT
132
132
MATCH PORT
MATCH PORT
260
260
COMPARING UNIT
COMPARING UNIT
COMPARING UNIT
COMPARING UNIT
263
261
RefB$_N$
RefB$_0$
RefA$_N$
RefA$_0$
215
225
227
273
271
WL0
WL1
WLM
S1
S2
SL1
SL2
MB$_0$
MB$_X$
MA$_0$
MA$_X$
101
102
103
142
142
INPUT CIRCUIT
DECODER
DECODER
MATCH CONTROLER

FIG. 2

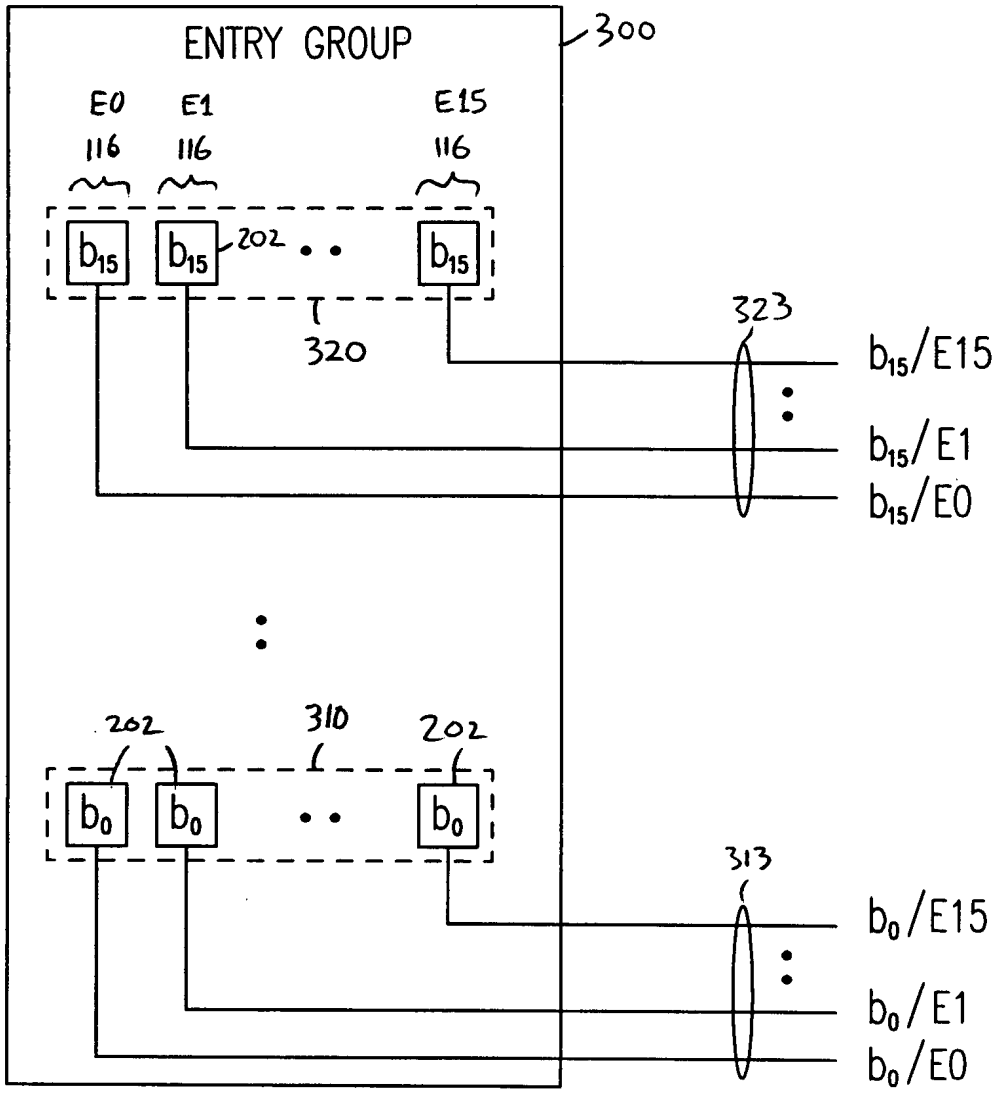

ENTRY GROUP
300
E0
E1
E15
116
116
116
b_{15}
b_{15}
202
b_{15}
320
323
$b_{15}/E15$
$b_{15}/E1$
$b_{15}/E0$
202
310
202
b_0
b_0
b_0
313
$b_0/E15$
$b_0/E1$
$b_0/E0$

FIG. 3

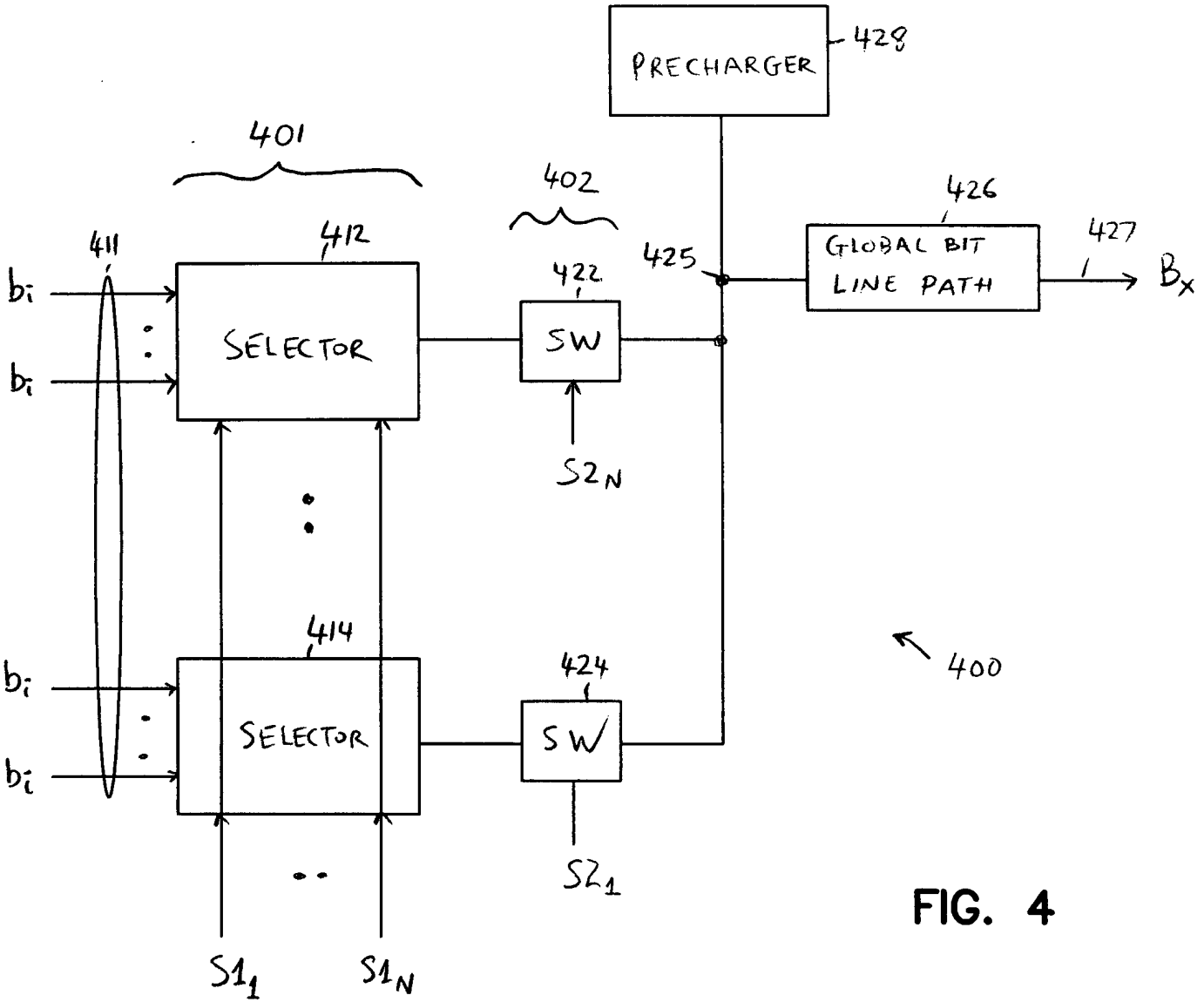
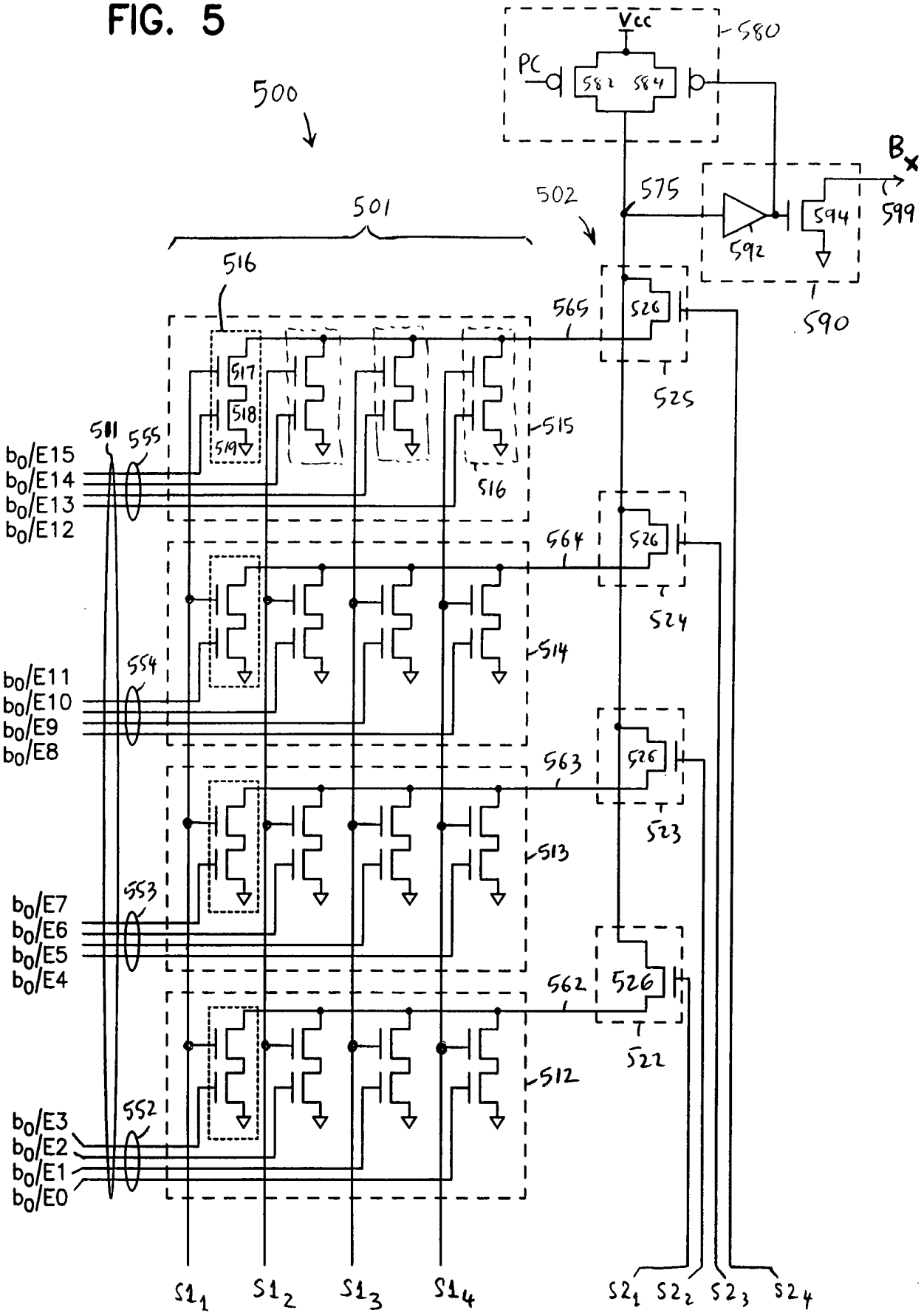

PRECHARGER
428
401
402
426
411
412
425
GLOBAL BIT LINE PATH
427
B_x
422
b_i
b_i
SELECTOR
SW
$S2_N$
414
424
400
b_i
b_i
SELECTOR
SW
$S2_1$
$S1_1$
$S1_N$

FIG. 4

FIG. 5


500
501
502
Vcc
580
PC
582
584
575
592
594
599
590
516
565
526
525
517
518
519
515
511
555
b0/E15
b0/E14
b0/E13
b0/E12
564
524
514
554
b0/E11
b0/E10
b0/E9
b0/E8
563
523
513
553
b0/E7
b0/E6
b0/E5
b0/E4
562
522
512
552
b0/E3
b0/E2
b0/E1
b0/E0
S1 1
S1 2
S1 3
S1 4
S2 1
S2 2
S2 3
S2 4

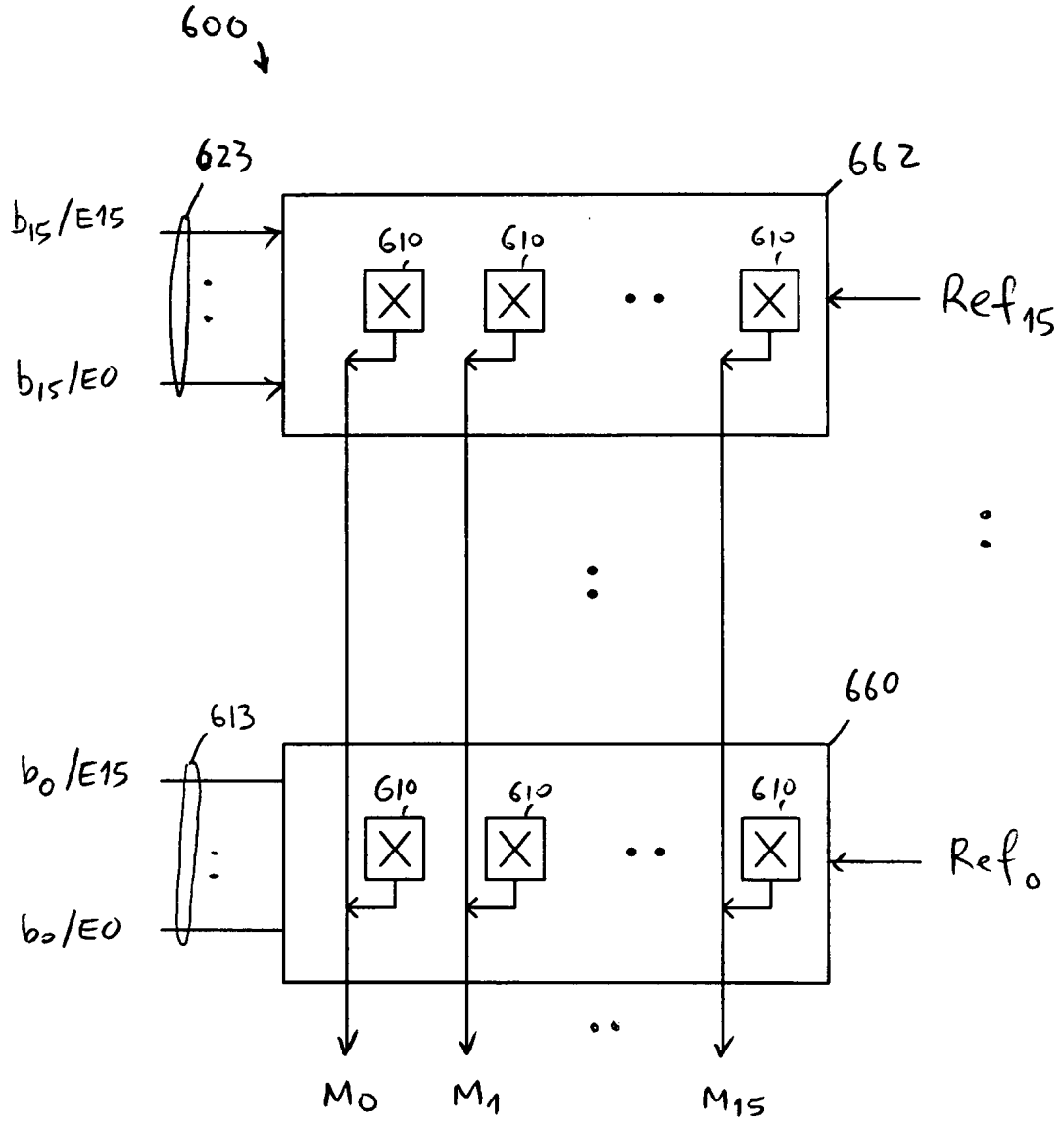

600
623
662
$b_{15}/E15$
$b_{15}/E0$
610
610
610
Ref_{15}
660
613
$b_0/E15$
$b_0/E0$
610
610
610
Ref_0
M_0
M_1
M_{15}

FIG. 6

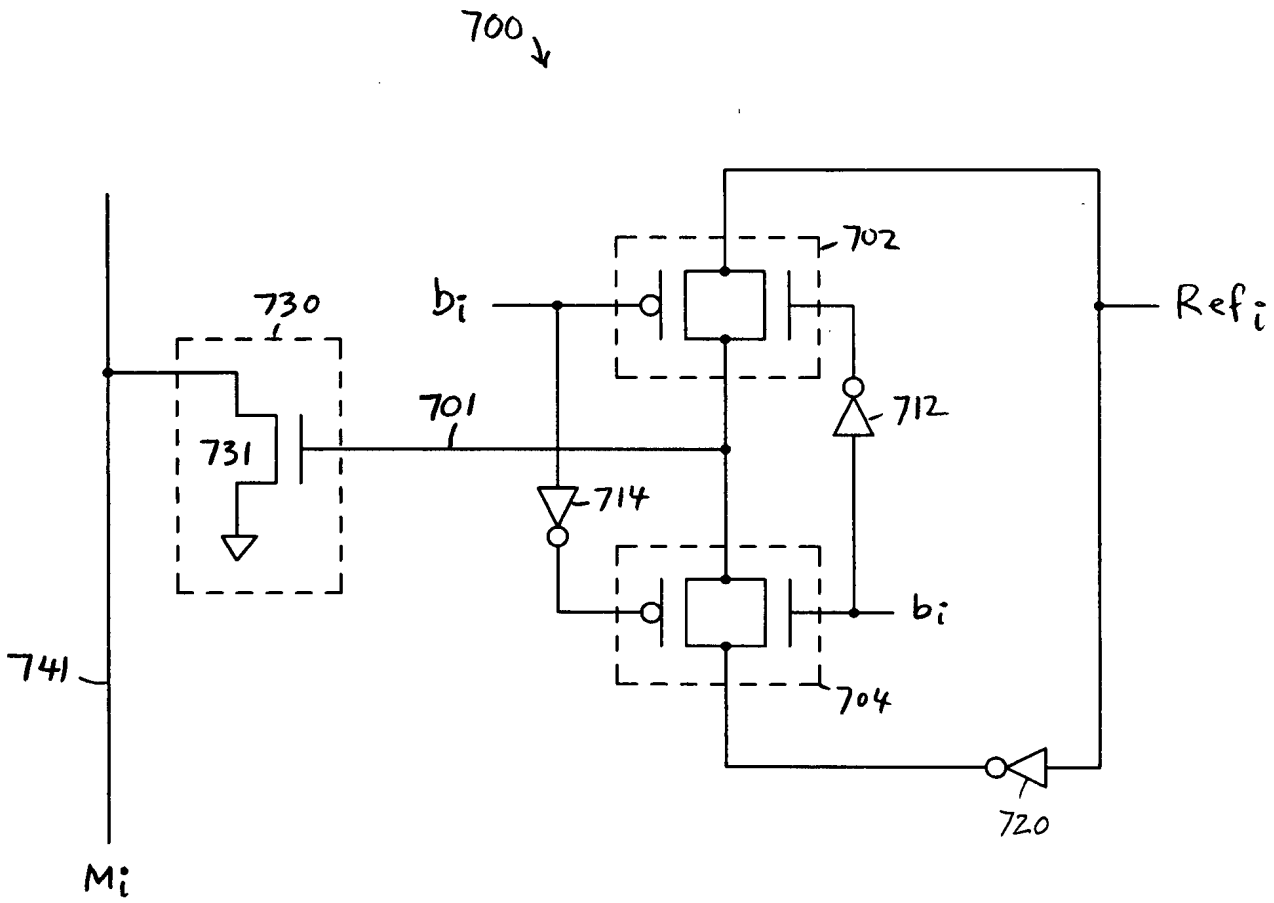


FIG. 7

b_i	Ref$_i$	Node 701	M_i
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

FIG. 8

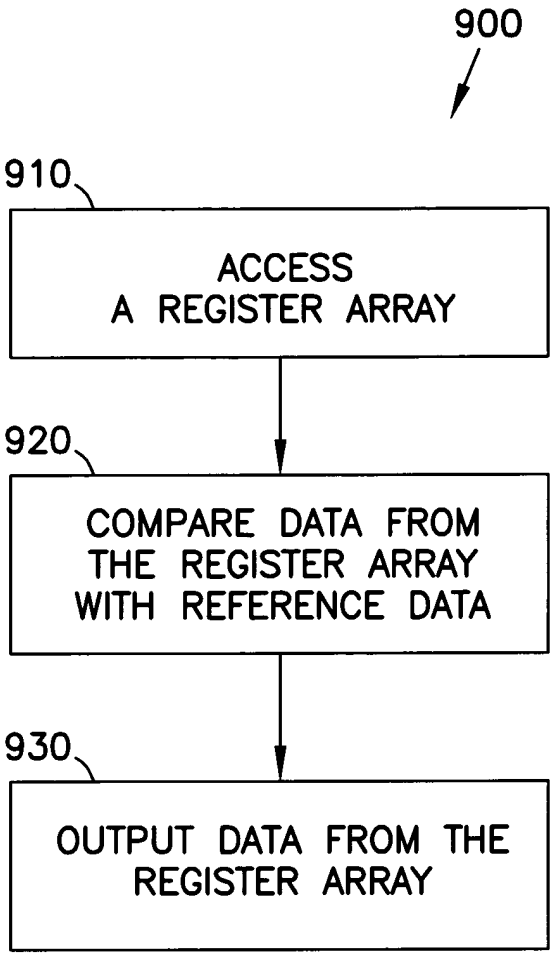

900
910
ACCESS A REGISTER ARRAY
920
COMPARE DATA FROM THE REGISTER ARRAY WITH REFERENCE DATA
930
OUTPUT DATA FROM THE REGISTER ARRAY

FIG. 9

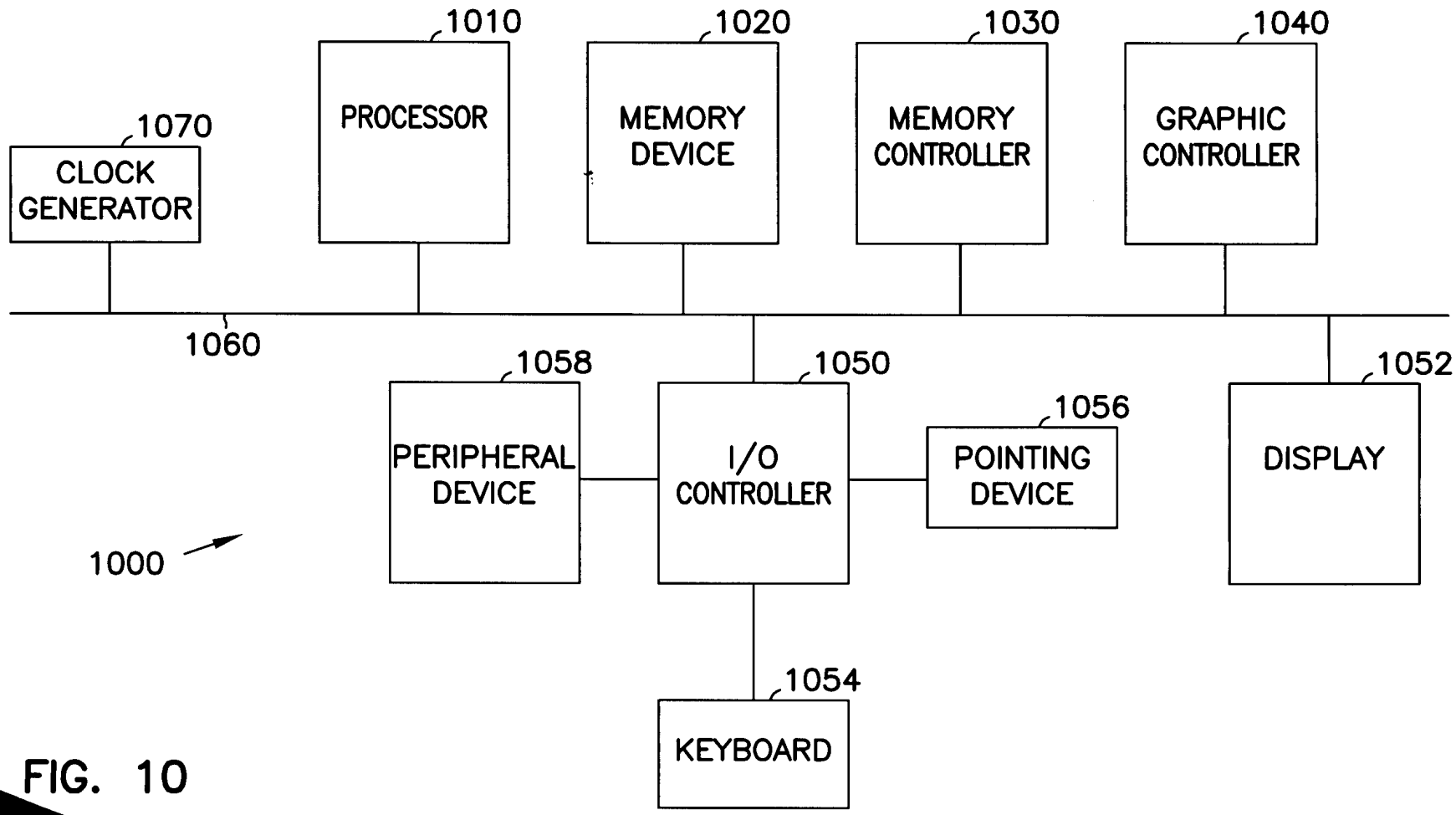

1010
PROCESSOR
1020
MEMORY DEVICE
1030
MEMORY CONTROLLER
1040
GRAPHIC CONTROLLER
1070
CLOCK GENERATOR
1060
1058
PERIPHERAL DEVICE
1050
I/O CONTROLLER
1056
POINTING DEVICE
1052
DISPLAY
1000
1054
KEYBOARD

FIG. 10